Electronic Materials

©2012 IEEE. REPRINTED, WITH PERMISSION, FROM

Next Generation Electroplating Technology for High Planarity, Minimum Surface Deposition Microvia Filling

† Ming-Yao Yen, †Ming-Hung Chiang, †Hsu-Hsin Tai, †Hsien-Chang Chen, *Kwok-Wai Yee, *Crystal Li, ‡ Mark Lefebvre, and ‡ Martin Bayes

Dow Electronic Materials, The Dow Chemical Company

IMPACT Conference Proceedings, October 2012.

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Dow Electronic Materials' products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

Electrolytic copper microvia filling is an enabling technology, prominently used in today's manufacture of HDI and packaging substrate applications for better reliability, increased circuit densification, design flexibility and thermal management. To meet these needs, seemingly incompatible objectives must be met. Thinner and more uniform surface copper deposits have to be produced; increasingly difficult microvia geometries must be filled, while maintaining plating rates capable of delivering production throughputs.

This paper describes a new pattern-plate, direct current (DC) copper electroplating process designed for packaging substrate applications. Microvia filling performance, surface distribution, trace profile and product reliability as a function of a variety of chemical and physical processing variables is discussed.

INTRODUCTION

Recently, the filling of microvias by copper electroplating has become a popular topic in the field of fabrication of printed circuit boards (PCBs) with high density interconnection [1] and IC substrate packages.

In order to produce the increasingly narrow line widths and spacing (L/S) required to route state of the art packages, build-up technology [2] is undergoing a shift from subtractive techniques towards Semi-Additive Process (SAP). This shift is being driven by the inherent limitations of subtractive processes etch resolution.

In Semi-Additive processing of build-up dielectrics, a photoresist pattern is formed after initial electroless metallization of the dielectric material. Following electroplating and resist stripping, the use of a "differential etching" process allows feature formation without the uses of a metal etch resist.

A modified SAP process, also referred to as Advanced-Pattern Process, is often used in HDI fabrication. In this case, a laminate coated with a thin copper foil is used for the starting material, rather than a bare dielectric.

Both the Semi-Additive and the Advanced Pattern Process are preferred over subtractive approaches due to their improved etch capability at feature dimensions below 40 microns.

COPPER ELECTROPLATING

The vast majority of electroplating baths used in PCB fabrication are based on electrolytes composed of copper sulfate and sulfuric acid. Owing to the low cost and the convenient operation, these sulfates based systems area well-established technology, and have been widely used in the PCB industry for over fifty years.

Inorganic Components

There are three inorganic components in an acid sulfate electrolyte: copper sulfate is the primary source of cupric ions, sulfuric acid primarily accounts for solution conductivity, and chloride ion acts as a co-suppressor. For packaging substrate applications, combining filled micro vias with a flat trace and pad profile exhibiting low convexity is critical.

Electrolytes optimized for micro via filling require high copper concentrations. As a result, these baths must contain lower acid concentrations for copper solubility. Electrolytes optimized for a flat trace and pad profile normally contain lower copper concentrations and higher concentrations of acid.

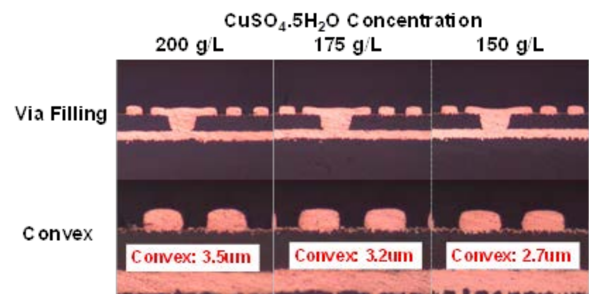

Figure 1. Via fill and typical line/trace profiles as a function of $CuSO_4.5H_2O$ concentration (at 2.0 ASD and 12µm plated copper thickness)

The compositions of via filling baths which must also plate through holes are slightly adjusted from the ideal compositions for via filling performance, so as to achieve sufficient through hole throwing power. Figure 1 shows the effect of copper sulfate concentration on via filling performance and trace profile.

Organic Components

Organic additives are used to refine and control the deposit characteristics in an acid sulfate system, and play a key role in promoting through hole filling behavior. Deposits made from acid sulfate electrolytes without these additives exhibit poor physical properties. In addition to enabling through hole filling behavior, organic additives are employed to improve grain refinement, throwing power, leveling and brightening of the deposit.

Carriers, also referred to as suppressors, are typically large molecular weight polyoxy-alkyl type compounds. Carriers are adsorbed at the surface of the cathode and in concert with chloride ion act to suppress [3] the plating rate.

Brighteners, also referred to as accelerators, are typically organo-sulfur compounds [4-5] that increase the plating reaction by displacing adsorbed carrier. Brightener compounds may exist in several forms in electrolytic working baths.

Levelers are typically nitrogen bearing heterocyclic or non-heterocyclic aromatic compounds that act by displacing brightener species in high current density sites (protrusions). Adsorption of these additives at protrusions reduces the plating rate in those regions.

PRODUCTION EQUIPMENT

With conventional vertical batch electroplating systems, increased production throughput may be realized by increasing the number and/or the size of the plating cells. When the size of a plating cell is increased, the number of panels within the cell increases proportionally. Depending on the specific design and dimensions of the plating cell, panels may be placed in either single or multiple rows on a flight bar. Unfortunately, increased panel loading tends to decrease plating uniformity, particularly when comparing panels from the center of the flight bar with those from the ends.

In contrast, the use of either horizontal or vertical conveyorized equipment promotes increased panel to panel consistency, as each panel "sees" the same overall flow and current distribution as it passes through the equipment. The improvements in consistency can be seen in both better surface thickness distribution and enhanced uniformity of throwing power and via filling, both within a panel and from panel to panel. Vertical In-Line plating (VIL) systems have been shown to give plating uniformity ≤ 5.0% coefficient of variation (CV) across 18" x 24" panels.

However, when side to side variation within a panel is considered, vertical continuous systems hold a significant advantage over horizontal systems, in that only vertical systems allow the 2 sides of the panel to be processed in effectively identical physical environments. Vertical In-line plating equipment designs are particularly suitable for via filling applications, as the vertical panel orientation minimizes air entrapment, and associated skipped or partially filled vias. In contrast, these defects can be problematic on the bottom side of panels processed in horizontal equipment.

Conveyorized systems have an overwhelming advantage over conventional vertical batch systems when it comes to handling thin core material. For ultra thin material, horizontal systems may hold a slight handling advantage over VIL plating systems.

When system cost and footprint are considered, VIL equipment affords considerable advantages versus horizontal designs of similar capacity. Additionally, more advanced multiple tracks VIL equipment designs are now available, which provide the capability for both conventional conformal plating and via filling capability within a single process line in addition to increased production throughput.

A wide variety of system design features that further enhance via filling performance may be incorporated in VIL plating equipment. These include the use of insoluble anodes and engineered fluid delivery devices such as eductors or nozzles designed to create impinging flow on panel surfaces. Insoluble anodes improve plating uniformity by presenting a more stable anode profile over time than copper anodes. Coupled with increased solution flow, insoluble anodes also allow the use of higher operating current densities.

EFFECT OF MASS TRANSPORT AND CURRENT DENSITY ON PLATING

Mass transport and current density have a significant impact on microvias filling capability [6]. In general, lower levels of solution flow were found to improve via filling performance. However, this improvement comes at the price of increased risk of improper fill in smaller diameter through holes (75 µm) and on thicker substrates 30 µm). Improper fill may lead to defects such as "seams" and voids within the plated deposit. The consequence of this behavior is that solution flow must be carefully chosen to achieve the best balance between levels of fill and plating quality for the specific applications being run.

The effects of current density are somewhat less complex. Lower current density will both enhance via filling performance and also produce product with lower levels of improperly filled vias. However, the impact of current density is strongest at the very early stages of via filling. Once vias have been partially filled, the current density may be raised without adverse effects.

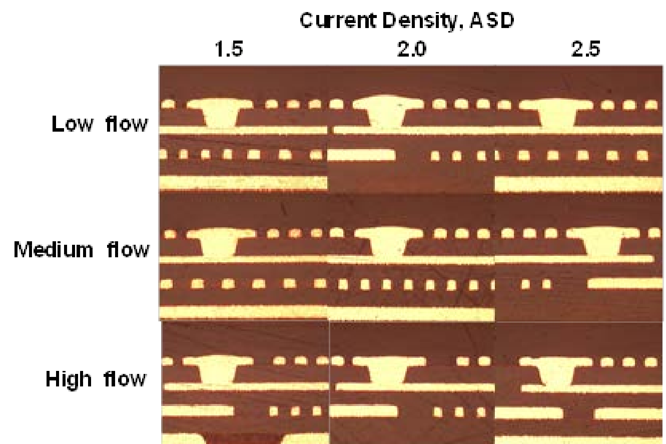

Figure 2. Filling performance of 75 µm diameter x 30 µm deep microvias as a function of solution flow rate and current density (12µm plated copper thickness)

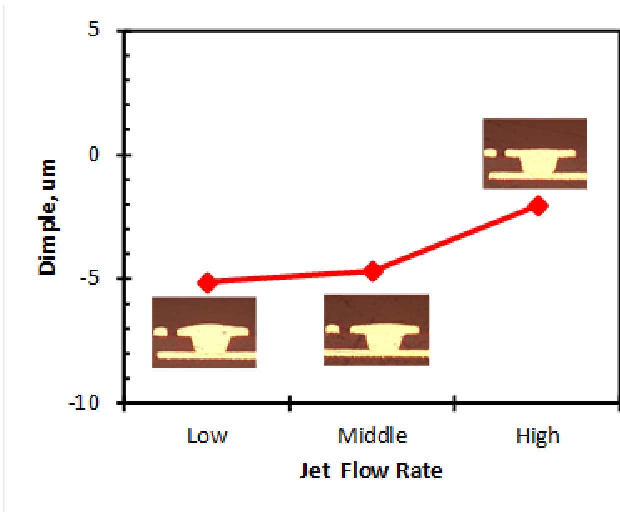

Figure 3. Via fill as a function of jet flow rate

PROCESS CAPABILITY – VIA FILL

Figure 4 shows the microvia fill evolution as a function of copper electroplating thickness using the novel plating formula. It is evident that, even when the plating thickness has only reached 5µm, significant bottom-up deposition is observed. Figure 5 shows the via fill performance for location to location filling consistency within an 18" x 24" panel.

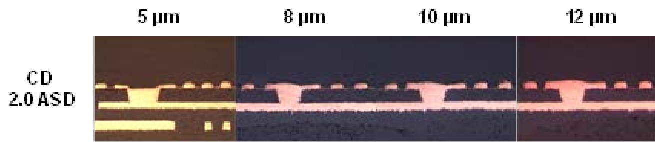

Figure 4. Via fill as a function of deposition thickness (for 75µm diameter x 30µm deep via)

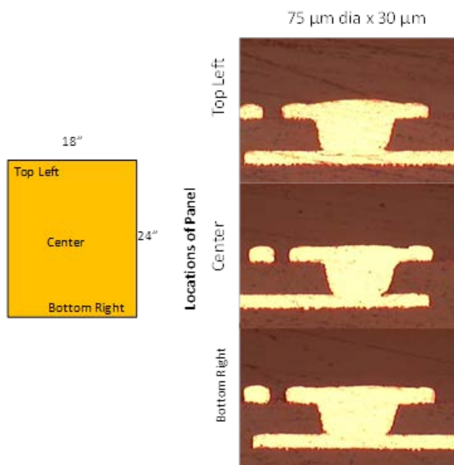

Figure 5. Via fill consistency across an 18" x 24" panel.

Figure 6 shows the typical line/trace profiles that can be achieved with the novel via fill chemistry. These profiles show excellent planarity.

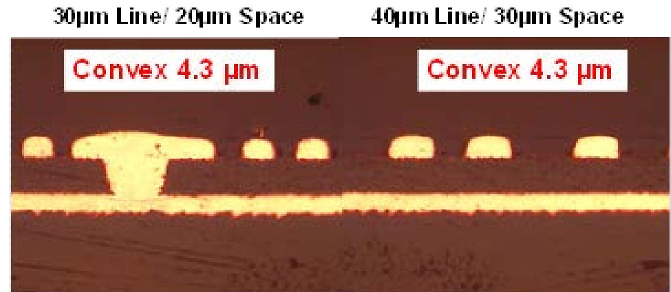

Figure 6. Effect of trace width and space on profile (at 2.0 ASD and 12µm plated copper thickness)

Figure 7 shows the surface of plated parts with filled microvias after selective etching. The resulting copper surface exhibits a normal increase in roughness without localized pitting.

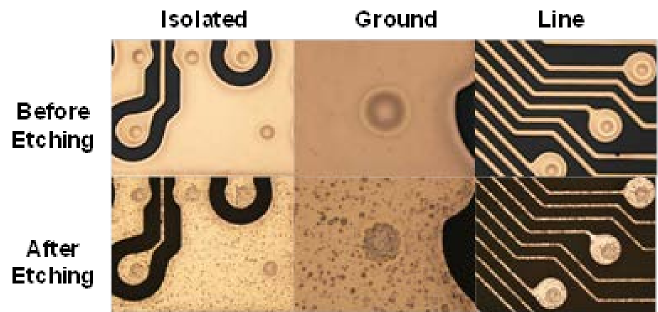

Figure 7. Via fill as a function of feature location and density after selective etching of the surface (75 µm x 100 µm vias, 2.0 ASD

PHYSICAL PROPERTIES AND RELIABILITY

Copper filled microvias exhibit excellent reliability. A solid plug of copper is inherently reliable and highly conductive. Table 1 shows the consistency of deposit physical properties as a function of current density.

Current Density ASD	Tensile Strength kpsi	Deposit Elongation %
0.6	41.4	22.6
1.0	42.6	24.9
1.5	43.1	21.9
20	44.5	21.1

Table 1. Deposit physical properties as a function of current density.

The impact of bath aging on microvia filling performance is shown in Fig. 8.

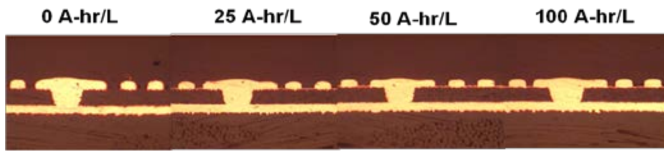

Figure 8. Via fill performance as function of bath age

Test panels were processed in a production scale plating cell at bath ages from 0 to more than 100 A.hr/L. Consistent via fill was maintained throughout the test. Table 2 shows the excellent deposit performance from a bath cycled in excess of 100 A.h/L.

Bath Age A-hr/L	**Number of defects /Number of vias**	**Cross sections of 75 µm dia x 30 µm deep vias**
0	0/50	
25	0/50	
50	0/50	
100	0/50	

Table 2. Via fill solder float performance as a function of bath age (5 cycles x 10 sec, 288 °C)

SUMMARY

The combination of specialized equipment and new copper via fill chemistry offers end users a cost effective, highly capable and production proven process for IC package substrate microvias filling.

A new, insoluble anode, DC microvia fill system is now available for high volume manufacturing (HVM), offering additional operating flexibility and end user preference.

REFERENCES

[1] K. Takagi, H. Honma, and T. Sasabe, IEEE Electr. Insul. Mag. (USA), 19, 27 (2003)

[2] T. Kobayashi, J. Kawasaki, K. Mihara, and H. Honma, Electrochim. Acta, 47, 85 (2001)

[3] M. Yokoi, S. Konishi, and T. Hayashi, Denki Kagakuoyobi Kogyo Butsuri Kagaku, 52, 218 (1984)

[4] T. P. Moffat, D. Wheeler, and D. Josell, Journal of The Electrochemical Society, C262-C271, 151, (2004)

[5] J. P. Healy, D. Pletcher, and T.H. Bailey, Journal of Electroanalytical Chemistry, 338, 25 (1998)

[6] M. Lefebvre, G. Allardyce, M. Seita, H Tsuchida, M. Kusaka, S. Hayashi, Circuit World, 9 , 29, 2 (2003)